60V N-Ch Power MOSFET

V_{DS}		60	V
$R_{DS(on),typ}$	V_{GS}=10V	6.7	m :
$R_{DS(on),typ}$	V_{GS}=4.5V	9.5	m :
$I_{D\ (Sillicon\ Limited)}$		44.6	A
$I_{D\ (Package\ Limited)}$		40	A

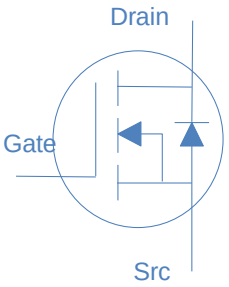
Feature

- High Speed Power Switching, Logic Level
- Enhanced Avalanche Ruggedness
- 100% UIS Tested 100% Rg Tested
- Lead Free, Halogen Free

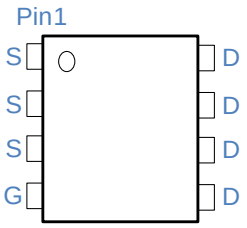
Application

- Hard Switching and High Speed Circuit
- DC/DC In Telecoms and Industrial

DFN3.3x3.3



Part Number	Package	Marking
HGM079N06SL	DFN 3.3*3.3	GM079N06L



Absolute Maximum Ratings at T_j=25 (unless otherwise specified)

Parameter	Symbol	Conditions	Value	Unit
Continuous Drain Current (Silicon Limited)	I_D	T_C=25	44.6	A
		T_C=100	28	
Continuous Drain Current (Package Limited)		T_C=25	40	A
Drain to Source Voltage	V_{DS}	-	60	V
Gate to Source Voltage	V_{GS}	-	±20	V
Pulsed Drain Current	I_{DM}	-	270	A
Avalanche Energy, Single Pulse	E_{AS}	L=0.3mH, T_C=25	60	mJ
Power Dissipation	P_D	T_C=25	30	W
Operating and Storage Temperature	T_J, T_{stg}	-	-55 to150	

Absolute Maximum Ratings

Parameter	Symbol	Max	Unit
Thermal Resistance Junction-Ambient	$R_{\theta JA}$	50	/W
Thermal Resistance Junction-Case	$R_{\theta JC}$	4.1	/W

Electrical Characteristics at T_j=25 (unless otherwise specified)

Static Characteristics

Parameter	Symbol	Conditions	Value			Unit
			min	typ	max	
Drain to Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS}=0V, I_D=250 PA	60	-	-	V
Gate Threshold Voltage	$V_{GS(th)}$	V_{GS}=V_{DS}, I_D=250 PA	1.0	1.8	2.4	
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS}=0V, V_{DS}=60V, T_j=25	-	-	1	PA
		V_{GS}=0V, V_{DS}=60V, T_j=100	-	-	100	
Gate to Source Leakage Current	I_{GSS}	V_{GS}=±20V, V_{DS}=0V	-	-	±100	nA
Drain to Source on Resistance	$R_{DS(on)}$	V_{GS}=10V, I_D=20A	-	6.7	7.9	m :
		V_{GS}=4.5V, I_D=16A	-	9.5	11.8	
Transconductance	g_{fs}	V_{DS}=5V, I_D=20A	-	26	-	S
Gate Resistance	R_G	V_{GS}=0V, V_{DS} Open, f=1MHz	-	1.5	-	:

Dynamic Characteristics

Input Capacitance	C_{iss}	V_{GS}=0V, V_{DS}=30V, f=1MHz	-	1620	-	pF
Output Capacitance	C_{oss}		-	415	-	
Reverse Transfer Capacitance	C_{rss}		-	3	-	
Total Gate Charge	Q_g(10V)	V_{DD}=30V, I_D=20A, V_{GS}=10V	-	24	-	nC
	Q_g(4.5V)			12		
Gate to Source Charge	Q_{gs}		-	5.0	-	
Gate to Drain (Miller) Charge	Q_{gd}		-	3.0	-	
Turn on Delay Time	$t_{d(on)}$	V_{DD}=30V, I_D=20A, V_{GS}=10V, R_G=10 : ,	-	9	-	ns
Rise time	t_r		-	4	-	
Turn off Delay Time	$t_{d(off)}$		-	29	-	
Fall Time	t_f		-	4	-	

Reverse Diode Characteristics

Diode Forward Voltage	V_{SD}	V_{GS}=0V, I_F=20A	-	0.9	1.2	V
Reverse Recovery Time	t_{rr}	V_R=30V, I_F=20A, $d_{IF/dt}$=300A/ Ps	-	30	-	ns
Reverse Recovery Charge	Q_{rr}		-	43	-	nC

Fig 1. Typical Output Characteristics	Figure 2. On-Resistance vs. Gate-Source Voltage

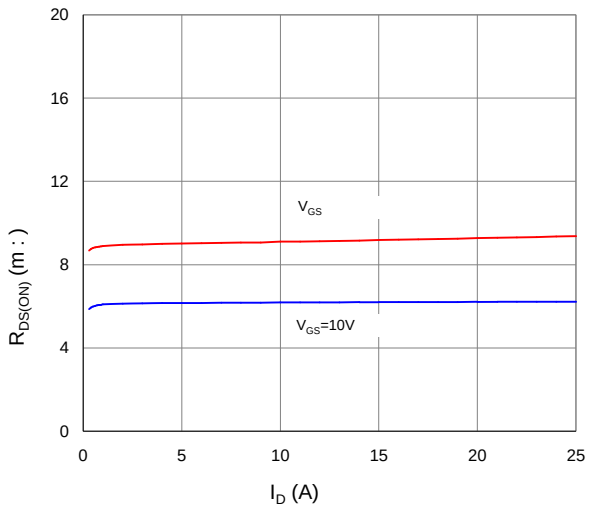
Figure 3. On-Resistance vs. Drain Current and Gate Voltage	Figure 4. Normalized On-Resistance vs. Junction Temperature
	

Figure 5. Typical Transfer Characteristics	Figure 6. Typical Source-Drain Diode Forward Voltage

Figure 7. Typical Gate-Charge vs. Gate-to-Source Voltage

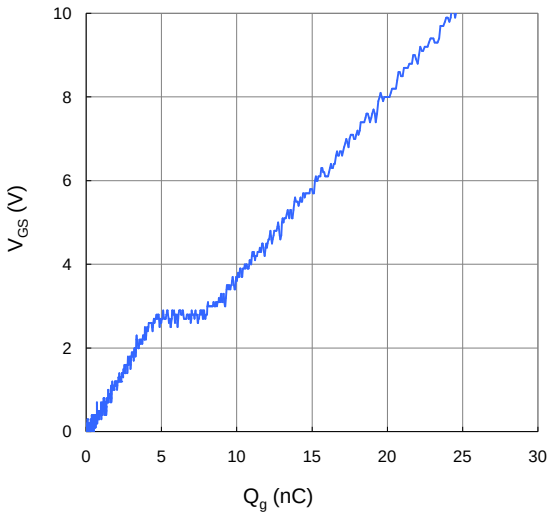


Figure 8. Typical Capacitance vs. Drain-to-Source Voltage

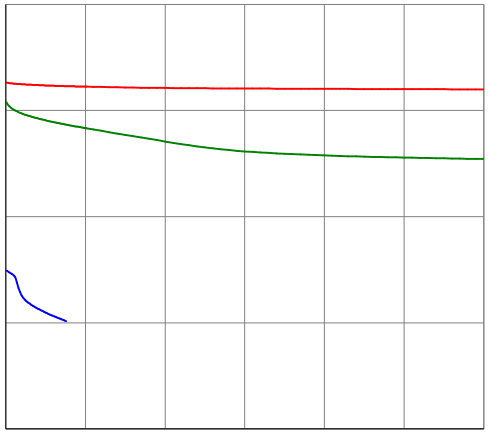


Figure 9. Maximum Safe Operating Area

Figure 10. Maximun Drain Current vs. Case Temperature

Figure 11. Normalized Maximum Transient Thermal Impedance, Junction-to-Ambient

Inductive switching Test

Gate Charge Test

Uclamped Inductive Switching (UIS) Test

Diode Recovery Test

Pac utline

DF P, 8 Leads